

ABSTRACT OF THE DISCLOSURE

A jitter generator produces a jittery test signal for use in performing a jitter test on an integrated circuit (IC) device under test (DUT). The jitter generator includes a programmable delay circuit for delaying a non-jittery input signal with a varying delay controlled by input digital delay control data to produce the test signal. A pattern generator supplies a sequence of delay control data to the programmable delay circuit causing it to produce a desired jitter pattern in the test signal. During a calibration process, a measurement unit feeds the test signal back to the input of the programmable delay circuit, causing the test signal to oscillate with a period proportional to the delay through the delay circuit. The measurement unit then measures the period of the test signal for various values of delay control data and reports measurement results. Based on the measurement results, host equipment then determines an appropriate sequence of delay control data for producing a desired jitter pattern in the test signal and programs the pattern generator to produce that sequence of delay control data during a jitter test. The jitter generator can form a part of a built-in, self-test (BIST) circuit implemented within the DUT itself.